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Martha Suarez[#1], Fabien Robert[#2], Geneviève Baudoin [#3], Martine Villegas[#4], Antoine Diet[*5]

[#] *Université Paris-Est, ESYCOM, ESIEE Paris*

2, Bd. Blaise Pascal - Cité Descartes BP99 - 93162 Noisy-le-Grand CEDEX, France

[1]suarezm@esiee.fr, [2]robertf@esiee.fr, [3]baudoing@esiee.fr, [4]villegam@esiee.fr

[*]*Département de Recherche en Electromagnétisme (DRE), Laboratoire des Signaux et Systèmes (L2S)*

UMR 8506. Supélec, plateau de Moulon, F-91192 Gif S/ Yvette, France

[2]antoine.diet@lss.supelec.fr

Abstract— **This study deals with high efficiency architectures enabling transmission of high PAPR signals. High PAPR signals result from new communication standards targeting high data rates and spectral efficiency. Polar Architectures, proposing the Envelope Elimination and Restoration (EER), code non constant envelope signals in order to obtain constant envelope signals and to use the power amplifier (PA) in switched mode. PA efficiency is affected by the signal coding and the frequency of the envelope modulator. First, this paper presents how the envelope binary distribution after coding affects the efficiency of a class E power amplifier. Then, the binary distribution of mobile WiMax signal is observed when it is coded with a Pulse Width Modulator in EER architecture and with a low pass Sigma-Delta Modulator in a polar architecture. This analysis yields to conclude on the influence of the coding technique on the class E amplifier efficiency and to estimate the efficiency that could be expected with both architectures.**

I. Introduction

Recent communication standards like the Long Term Evolution (LTE) and mobile WiMAX target high data rate transmission. They adopt advanced modulation schemes like Orthogonal Frequency Division Modulation (OFDM) and become more flexible in terms of channel bandwidths. Envelope variation can be described by the peak-to-average ratio (PAR) which is used as a guide to estimate the maximum linear power available from the Power Amplifier (PA). New communications standards signals can present high PAR which means that the PA must be backed off to operate linearly. Power amplifiers dissipate more dc power than any other circuit in the transmitter and their efficiency is critical for the whole transmitter architecture. In this context, the principle of switched mode PAs which offer very high efficiency for constant envelope signals becomes interesting to reduce power consumption of the transmitter. There are architectures enabling to transform the non-constant envelope signal into a constant one using for example Pulse Width Modulator (PWM) or low-pass Sigma Delta (ΣΔ) Modulator associated to switched mode amplifiers in class F or E [1]-[5].

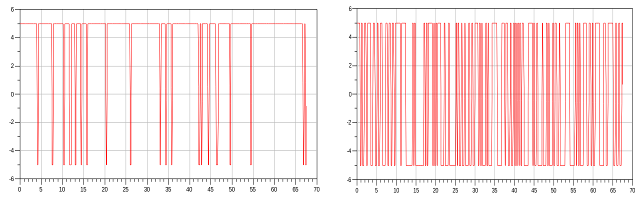
This paper focuses on the influence of the coded signal distribution on the efficiency of a class E power amplifier designed for Mobile WiMAX (3.7 GHz) [6]. It begins by considering different amplitude distribution levels of the PA input signal, as well as different coding frequencies. It then describes two constant envelope transforming methods: the EER/PWM architecture and the Polar ΣΔ architecture. Next, for a mobile WiMAX input signal, it presents the data distribution and probability density after coding the envelope whit these two architectures. The paper concludes by summarizing the efficiency that could be expected from the two considered architectures.

II. Input Signal Parameters Affecting the Efficiency of a Switched Power Amplifier

To optimize performances of the switched mode power amplifier (SMPA), it is necessary to study the shape of the signal to be amplified and the influence of the coding technique in the PA efficiency.

A. Pseudo-random distributed levels

This study assumes that the PA input signal has a binary shape. The polar architecture provides a coded envelope signal with a square shape and which levels may vary between “A” and “-A”. It is important to observe which proportion of “A” or “-A” levels provides the best switching conditions at the SMPA. Indeed by promoting a level over another will decrease the number of phase jumps around the carrier. Fig. 1 presents two binary frames, representing for the first a signal with 10% of “A” levels and for the second 50% of “A” levels.



(i) (ii)

Fig. 1 P(-A) = 10% (i) et 50% (ii)

B. Impact of the Minimum Time at an Amplitude Level

If T_{min} is defined as the minimum time of an amplitude level (“A” or “-A”), its value varies depending on the frequency coding used by the envelope modulator in the architecture. It has to be considered that a too fast change of state, does not allow optimal commutation. The higher the coding frequency is the higher phase jumps at the carrier appear. The next section illustrates the importance of T_{min} on capabilities of the SMPA to switch and to ensure maximum efficiency.

III. Influence of the Coded Signal on the Class E Amplifier Efficiency

A. *Design of the class E amplifier*

There are different classes of SMPAs (D, S, E and F), based on different transistor behaviors and reactive elements of the load network [7]-[9]. Class D and S are used in pulsed and low frequency applications. Class E and F are suitable for RF applications but Class F is based on several resonating networks with high Q factors difficult to implement. Class E PA, makes use of an inductor and a shunt capacitor which can absorb the parasitic output capacitance of the transistor. The topology used to design the class E amplifier is described in Fig. 2 and is named "serial inductor" [7].

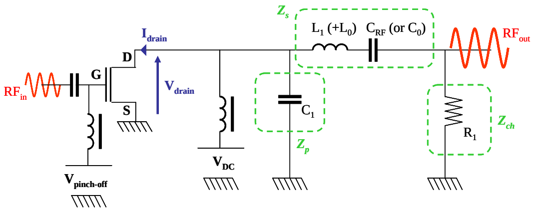


Fig. 2. Serial inductor topology of a Class E amplifier

A high efficiency SMPA is based on maximum voltage at zero current and vice versa, with no DC power dissipation. It's possible to calculate the optimum value of Class E output network element. In this case, the output of the transistor is supposed to be a short or an open circuit and the quality factor (Q) of C0-L0 is considered as infinite (perfect filtering conditions):

$$C_0 = \frac{1}{(Q-1.15249)\times Rload \times \omega_0}, \quad L_0 = \frac{1}{C_0\omega_0^2} \tag{1}$$

$$C_{shunt} = \frac{0.1836}{Rload \times \omega_0} - C_{DS} \tag{2}$$

$$L_{serial} = \frac{Rload \times 1.15249}{\omega_0} \tag{3}$$

As previously announced, the class E amplifier has been designed to operate at 3.7 GHz [6]. Input matching network has been designed keeping in mind that it should not filter the signal provided by the architecture. The goal is to preserve the constant envelope property. The designed amplifier offers a drain efficiency (η) of 86.4%, an overall efficiency (η_0) of 79.2% and 10,1dB gain as the input is an 8 dBm 1-tone signal. With a square signal at the same input power, the result is equivalent in terms of gain. Looking at efficiencies η and η_0 are 82% and 75.7% respectively.

B. *Analysis of performances depending on the coded signal*

Performances of the amplifier mainly lie in the observation of its ability to switch and provide power. Thus, the drain efficiency and gain are indicators of the impact of signal coding on the amplifier. Initially, the coded signal has been simulated by a binary square signal was modelled using a Bernoulli probabilistic distribution function over a 10000 bits frame. It then simulates the impact of a constant envelope signal with a binary shape, around a 3.7GHz carrier frequency on the designed PA. Simulations were done using Agilent ADS. It can be observed in Fig. 3 that the drain efficiency value (ηD) changes depending on the probability of "-A" levels. Different envelope coding frequencies values (f_{sd}) multiples of a carrier frequency centred at 3.7GHz have been considered. In any case, the frequency of the PA input signal is 3.7 GHz.

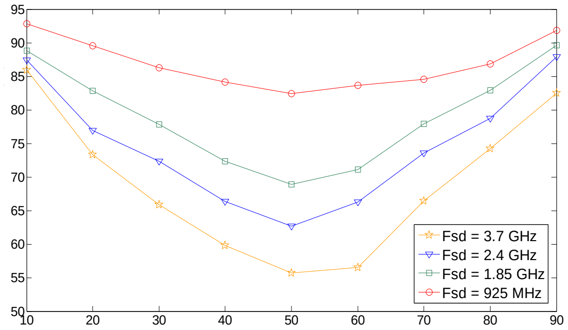


Fig. 3. η_D(%) function of P(-A).

When there is a high gap between the two amplitude levels, there is a real improvement of efficiency performances. Drain efficiency is mainly degraded when the number of "A" levels is equal to "-A" levels. In this configuration the signal has the maximum of phase jumps and switching conditions are degraded. In the cases where f_{sd} is equal to 3.7GHz, the variation of efficiency reaches 30% between the best and the worst level distributions. The best performance is obtained for f_{sd} equal to a quarter of the carrier and a probability P(-A) of 10 or 90%. Thus, we limit phase jumps and decrease the switching speed required by increasing the minimum time at a level (T_{min}).

C. *Improvements Considerations*

It is possible to improve the PA performances by making packets of bits, in that case the same data distribution of the levels is kept but the T_{min} is increased. Fig. 4 presents the effect of grouping bits of same level into packets.

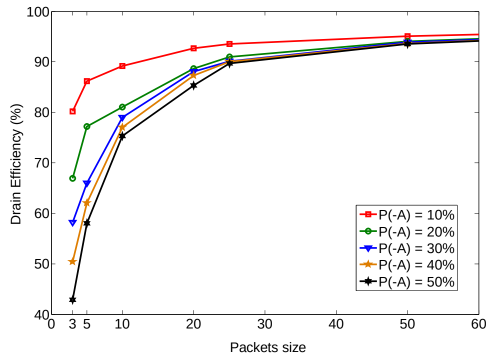


Fig. 4. η_D(%) for different packets sizes.

Simulations were conducted using frames of 10000 bits. Independently of the “A” or “-A” levels probability, there is a convergence of performances when the packets size increases. The longer packets are, the less straighten are switching conditions. The number of successive bits at the same level value depends of the packets size. Fig.5 shows a focus of packets size around an average value. This leads to artificially reduce the switching speed and is equivalent to a reduction of the coding frequency under a Bernoulli distribution condition. For P(-A) = 50%, drain efficiency increases from 56% to 82% by making packets of 15bits. This method lead to obtain a T_{min} six times higher than the initial one, but at the same coding frequency.

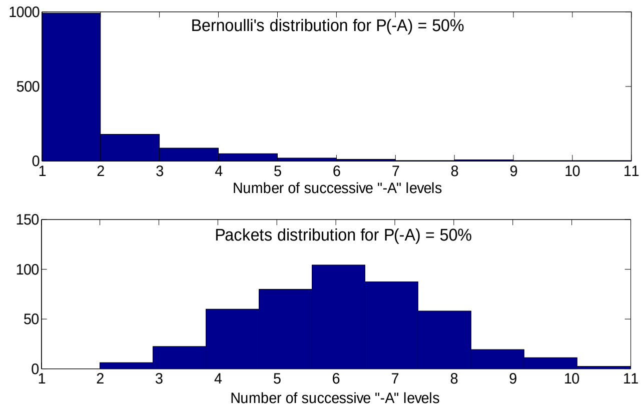


Fig. 5. Size of « +A » packets for f_{sd}=3.7GHz.

IV. Considered Constant Envelope Architectures

The two architectures presented in this section transform non constant envelope signals in constant envelope signals and are associated to high efficiency PA. They are polar architectures because they use different paths to transmit magnitude and phase of the complex transmit signal. In both cases, phase signal is modulated to the RF frequency by I/Q modulator or modulated PLL. Since the amplitude of the phase modulated signal remains constant, it could be directly applied to the drain of the class E amplifier. That’s the principle of the EER Architecture presented in Fig.6.

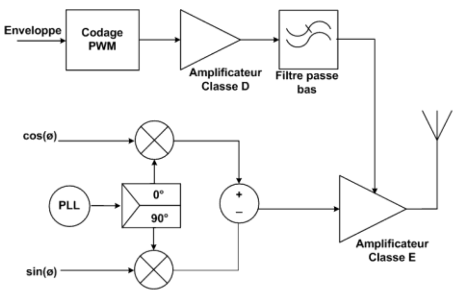


Fig. 6 EER / PWM Transmitter Architecture

Envelope information is coded using a PWM modulator and then restored by supply modulation or multiplying directly the driving signal of the PA [1]. At the output of the PWM modulator, the signal has constant envelope and may vary between [0, A] if restoration is done by supply modulation (Fig.6) or between two amplitude levels [-A, A] if multiplying the phase.

In the polar ΣΔ architecture, presented in Fig. 7, the envelope is coded using a 1 bit low-pass ΣΔ modulator and the envelope restoration is accomplished before the amplification [2]. As showed in the Fig. 7, the envelope at the output of the ΣΔ modulator has two amplitude levels [-A, A].

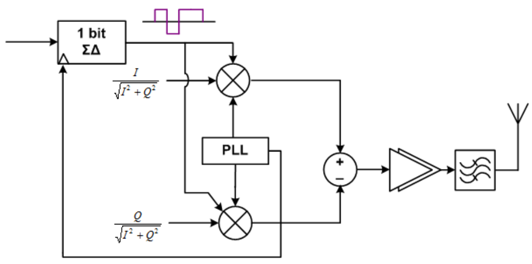


Fig. 7 Polar ΣΔ Architecture

A band-pass filter is required at the output of the PA in order to filter the quantization noise shaped by the ΣΔ modulator.

V. Output Signals Distribution

A mobile WiMAX signal at 3.7 GHz has been used to compare the packets distribution at the output of the PWM and ΣΔ modulators. According to WiMAX forum implementation profiles, a 10 MHz channel was considered including 1024 carriers modulated by 64-QAM.

A. *Polar Sigma-Delta Architecture*

Sigma Delta modulator oversamples the input signal and accomplish a noise shaping. ΣΔ frequency (f_{sd}) must be chosen high enough compared to the signal bandwidth in order to reduce noise in the band and obtain high signal to noise ratio (SNR). Carrier frequency (f_c) has to be higher than f_{sd} to avoid noise overlapping after RF modulation. Simulations were conducted assuming f_{sd} = f_c. Modulator order is directly related to the better noise shaping and SNR, but at the same time, low order modulators are less susceptible to limit cycles, easier to implement and offer high stability [10]. An order 2 modulator has been chosen for simulations. ΣΔ modulator is low-pass and has a feedback structure.

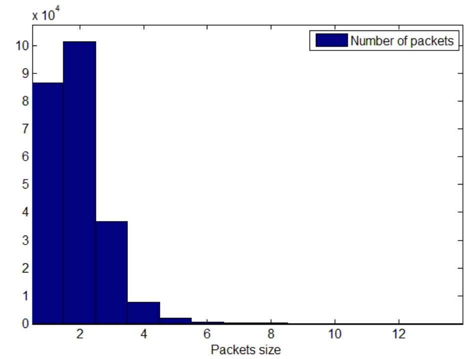


Fig. 8 Packets Histogram of the Polar ΣΔ architecture

At the ΣΔ modulator output signal varies between [-1, 1], the “-1” level appears with a probability close to 37% and “1” level with a probability close to 63%. Packets distribution histogram at the output of the ΣΔ modulator is presented in Fig.8. It has been computed counting the number of times each "1" level was repeated in the ΣΔ output signal. The minimum time of an amplitude level (T_{sd}) is constant and depends on the ΣΔ modulator frequency (f_{sd}).

B. EER Architecture with Pulse Width Modulator

Typically, PWM modulator frequency (f_{pwm}) is not as elevated as the ΣΔ modulator frequency. For simulations purposes and aiming to compare results with both architectures, f_{pwm} has been chosen to be a multiple of f_{sd} (370 MHz). PWM minimum time (T_{pwm}) has been initially fixed to be the same as the ΣΔ output minimum time (T_{sd}). The PWM modulator output signal varies between [-1, 1], the "-1" level appears with a probability close to 69% and "1" level with a probability close to 31%. Packets distribution histogram at the output of the PWM modulator is presented in Fig.9.

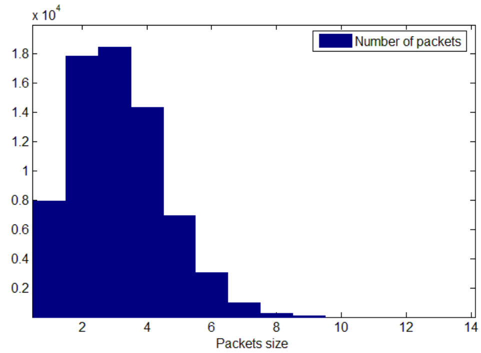


Fig. 9 Packets Histogram of the EER architecture

VI. Analysis And Comparison

Levels distributions at the output of the ΣΔ and PWM modulators are not the same. For the first one the "-1" probability is close to 37% while for the second one is close to 69%. According to Fig.3, for the same minimum time (T_{pwm} = T_{sd}) the drain efficiency that could be expected is similar for the two modulators, between 60 – 65%. On the other hand, the minimum time at the output of the PWM modulator (T_{pwm}) is not constant as with the ΣΔ modulator, and of course, T_{pwm} could be shorter than T_{sd}. This means that the amplifier should support faster variations in the input signal than with the ΣΔ modulator.

Another simulation with T_{pwm} ten times shorter than T_{sd} has been conducted (T_{pwm} = T_{sd} /10). Obtained results are presented in Fig. 10. Fig. 10 confirms Fig. 8 and Fig. 9 results and shows that the PWM output follows a Rayleigh distribution. Levels shorter than T_{sd} could appear with a probability of about 15%. Fig. 10 also shows that PWM modulator generates longer packets than ΣΔ, which according to Fig. 4 increases the PA efficiency. Mean size of PWM packets is 3 (2.8 for T_{min} = T_{sd}/10 and 3.1 for T_{min} = T_{sd}) and mean size of ΣΔ packets is 2. According to Fig. 4 expected efficiency for PWM modulator is about 58% (P(-A) = 70% symmetrical to P(-A) = 30%) while it's less than 50% for the ΣΔ modulator (P(-A) = 40%). ΣΔ modulator output presents then more phase jumps (smaller packets) than PWM modulator which does not provides the best switching conditions at the SMPA.

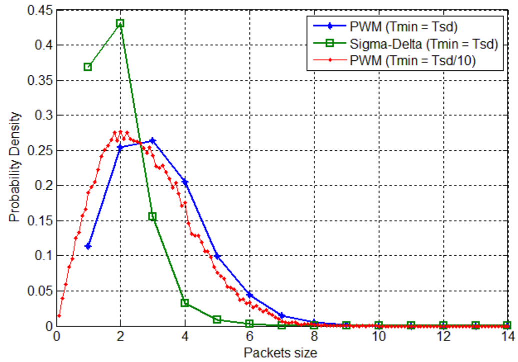


Fig. 10 Packets Histogram of the EER architecture

VII. Conclusions

This paper studied, in polar architectures, the influence of the envelope coding technique on the class E amplifier efficiency. PWM and ΣΔ modulators have been considered. It has been demonstrated by simulations that the drain efficiency is affected by the probability of each amplitude level at the output of the modulator but also by the way the amplitude levels are grouped (packets). Expected efficiency of the PWM envelope modulator architecture is higher because of the higher amplitude probability gap and larger packets size. Trade-off of the PWM modulator architecture is that PA could be required to switch faster than with the ΣΔ modulator.

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